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CLAIMS

WHAT IS CLAIMED:

1. A device, comprising:

a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said transistor being comprised of a gate electrode, said bulk substrate being doped with a dopant material at a first concentration level; and

a first doped region formed in said bulk substrate, said first doped region being comprised of a dopant material that is the same type as said bulk substrate dopant material, said first region having a greater concentration level of dopant material than said first concentration level, said first doped region being substantially aligned with said gate electrode.

2. The device of claim 1, further comprising second and third doped regions formed in said substrate, said second and third doped regions being comprised of a dopant material that is the same type as said bulk substrate dopant material, said second and third doped regions having a greater concentration level of dopant material than said first concentration level, said first doped region being vertically spaced apart from said second and third doped regions

3. The device of claim 1, wherein said transistor is comprised of at least one of an NMOS and PMOS device.

4. The device of claim 1, wherein said buried oxide layer is comprised of silicon dioxide and has a thickness ranging from approximately 5-50 nm.

5. The device of claim 1, wherein said active layer is comprised of silicon and has a thickness of approximately 5-30 nm.

6. The device of claim 1, wherein said gate electrode is comprised of polysilicon and has a thickness of approximately 100-150 nm.

7. The device of claim 2, wherein said gate electrode has a thickness and wherein said first doped region is vertically spaced apart from said second and third doped regions by a distance that corresponds approximately to said thickness of said gate electrode.

8. The device of claim 2, wherein said bulk substrate is doped with a P-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and said first, second and third doped regions are doped with a P-type dopant material at a dopant concentration of at least approximately 10^{16} ions/cm^3.

9. The device of claim 2, wherein said bulk substrate is doped with an N-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and said first, second and third doped regions are doped with an N-type dopant material at a dopant concentration of at least approximately 10^{16} ions/cm^3.

10. The device of claim 1, wherein said bulk substrate is doped with a P-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and said first doped region

is doped with a P-type dopant material at a dopant concentration of at least approximately 10^{16} ions/cm^3.

11. The device of claim 1, wherein said bulk substrate is doped with an N-type dopant material at a concentration of approximately 10^{15} ions/cm^3 and said first doped region is doped with an N-type dopant material at a dopant concentration of at least approximately 10^{19} ions/cm^3.

12. The device of claim 2, wherein said first, second and third doped regions each have a thickness of approximately 10-50 nm.

13. The device of claim 1, wherein said first doped region has a thickness of approximately 10-50 nm.

14. The device of claim 2, wherein each of said second and third doped regions has an inner edge that is approximately aligned with respect to said gate electrode.

15. The device of claim 1, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

16. The device of claim 2, wherein said second and third doped regions each have an upper surface that is positioned below an interface between the buried oxide layer and the bulk substrate by a distance that corresponds approximately to a thickness of the gate electrode.

17. The device of claim 1, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections.

18. A device, comprising:

a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said transistor being comprised of a gate electrode, said bulk substrate being doped with a dopant material at a first concentration level; and

first, second and third doped regions formed in said bulk substrate, said first, second and third doped regions being comprised of a dopant material that is the same type as said bulk substrate dopant material, said first, second and third doped regions having a greater concentration level of dopant material than said first concentration level, said first doped region being substantially aligned with said gate electrode and vertically spaced apart from said second and third doped regions.

19. The device of claim 18, wherein said transistor is comprised of at least one of an NMOS and PMOS device.

20. The device of claim 18, wherein said buried oxide layer is comprised of silicon dioxide and has a thickness ranging from approximately 5-50 nm.

21. The device of claim 18, wherein said active layer is comprised of silicon and has a thickness of approximately 5-30 nm.

22. The device of claim 18, wherein said gate electrode is comprised of polysilicon and has a thickness of approximately 100-150 nm.

23. The device of claim 18, wherein said gate electrode has a thickness and wherein said first doped region is vertically spaced apart from said second and third doped regions by a distance that corresponds approximately to said thickness of said gate electrode.

24. The device of claim 18, wherein said bulk substrate is doped with a P-type dopant material at a concentration level of approximately 10^{15} ions/cm^3 and said first, second and third doped regions are doped with a P-type dopant material at a dopant concentration level of at least approximately 10^{16} ions/cm^3.

25. The device of claim 18, wherein said bulk substrate is doped with an N-type dopant material at a concentration level of approximately 10^{15} ions/cm^3 and said first, second and third doped regions are doped with an N-type dopant material at a dopant concentration level of at least approximately 10^{16} ions/cm^3.

26. The device of claim 18, wherein said first, second and third doped regions each have a thickness of approximately 10-50 nm.

27. The device of claim 18, wherein each of said second and third doped regions has an inner edge that is approximately aligned with respect to said gate electrode.

28. The device of claim 18, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

29. The device of claim 18, wherein said second and third doped regions each have an upper surface that is positioned below an interface between the buried oxide layer and the bulk substrate by a distance that corresponds approximately to a thickness of the gate electrode.

30. The device of claim 18, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections.

31. A device, comprising:

a transistor formed above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said transistor being comprised of a gate electrode having a thickness, said bulk substrate being doped with a dopant material at a first concentration level; and

first, second and third doped regions formed in said bulk substrate, said first, second and third doped regions being comprised of a dopant material that is the same type as said bulk substrate dopant material, said first, second and third doped regions having a greater concentration level of dopant material than said first concentration level and at least a concentration level of approximately 10^{16} ions/cm^3, said first doped region being substantially aligned with said gate electrode and vertically spaced apart from said second and third doped regions

by a distance that corresponds approximately to said thickness of said gate electrode.

32. The device of claim 31, wherein said transistor is comprised of at least one of an NMOS and PMOS device.

33. The device of claim 31, wherein said buried oxide layer is comprised of silicon dioxide and has a thickness ranging from approximately 5-50 nm.

34. The device of claim 31, wherein said active layer is comprised of silicon and has a thickness of approximately 5-30 nm.

35. The device of claim 31, wherein said gate electrode is comprised of polysilicon and has a thickness of approximately 100-150 nm.

36. The device of claim 31, wherein said bulk substrate is doped with a P-type dopant material at a concentration level of approximately 10^{15} ions/cm^3 and said first, second and third doped regions are doped with a P-type dopant material at a dopant concentration level of at least approximately 10^{16} ions/cm^3.

37. The device of claim 31, wherein said bulk substrate is doped with an N-type dopant material at a concentration level of approximately 10^{15} ions/cm^3 and said first, second and third doped regions are doped with an N-type dopant material at a dopant concentration level of at least approximately 10^{16} ions/cm^3.

38. The device of claim 31, wherein said first, second and third doped regions each have a thickness of approximately 10-50 nm.

39. The device of claim 31, wherein each of said second and third doped regions has an inner edge that is approximately aligned with respect to said gate electrode.

40. The device of claim 31, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

41. The device of claim 31, wherein said second and third doped regions each have an upper surface that is positioned below an interface between the buried oxide layer and the bulk substrate by a distance that corresponds approximately to the thickness of the gate electrode.

42. The device of claim 31, further comprising a source region, a drain region, a sidewall spacer and a plurality of conductive interconnections.

43. A method, comprising:

forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level; and

performing an ion implant process using at least said gate electrode as a mask to implant a dopant material into said bulk substrate, said implant process being performed with a dopant material that is of the same type as said dopant

material in said bulk substrate, said implant process resulting in a first doped region formed in said bulk substrate that is substantially aligned with said gate electrode, said first doped region having a dopant concentration level that is greater than said first concentration level.

44. The method of claim 43, wherein forming a gate electrode comprises forming a gate electrode comprised of polysilicon.

45. The method of claim 43, wherein forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level, comprises forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate comprised of silicon, a buried oxide layer comprised of silicon dioxide and an active layer comprised of silicon, said bulk substrate being doped with a dopant material at a first concentration level.

46. The method of claim 43, wherein forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level, comprises forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a P-type dopant material at a first concentration level of approximately 10^{15} ions/cm^3.

47. The method of claim 43, wherein forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer,

said bulk substrate being doped with a dopant material at a first concentration level, comprises forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with an N-type dopant material at a first concentration level of approximately 10^{15} ions/cm^3.

48. The method of claim 43, wherein said first doped region has a dopant concentration level of at least approximately 10^{16} ions/cm^3.

49. The method of claim 43, wherein performing said ion implant process further forms second and third doped regions in said bulk substrate, said second and third doped regions having a dopant concentration level that is greater than said first concentration level, said first doped region being vertically spaced apart from said second and third doped regions.

50. The method of claim 43, wherein performing said ion implant process further forms second and third doped regions in said bulk substrate, said second and third doped regions having a dopant concentration level that is greater than said first concentration level, said first doped region being vertically spaced apart from said second and third doped regions by a distance that approximately corresponds to a thickness of said gate electrode.

51. The method of claim 43, wherein performing said ion implant process further forms second and third doped regions in said bulk substrate, said second and third doped regions each having an upper surface, said upper surface of each of said second and third doped regions being positioned below an interface between said buried oxide layer and said

bulk substrate by a distance that approximately corresponds to a thickness of said gate electrode.

52. The method of claim 43, wherein performing said ion implant process further forms second and third doped regions in said bulk substrate, said first doped region having an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate, said first doped region being vertically spaced apart from said second and third doped regions, said second and third doped regions each having an upper surface, said upper surface of each of said second and third doped regions being positioned below an interface between said buried oxide layer and said bulk substrate by a distance that approximately corresponds to a thickness of said gate electrode.

53. The method of claim 43, wherein performing said ion implant process results in said first doped region having a thickness of approximately 10-50 nm.

54. The method of claim 50, wherein performing said ion implant process results in said second and third doped regions each having a thickness of approximately 10-50 nm.

55. The method of claim 43, wherein performing said ion implant process comprises performing said ion implant process at an energy level ranging from approximately 40-400 keV.

56. The method of claim 43, wherein performing said ion implant process comprises performing said ion implant process with a dopant dose that ranges from approximately $1e^{14}$-$1e^{16}$ ions/cm^2.

57. The method of claim 43, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

58. The method of claim 43, further comprising performing at least one anneal process at a temperature ranging from approximately 600-1050°C after said ion implant process is performed.

59. The method of claim 43, further comprising forming a source region, a drain region and a plurality of conductive contacts.

60. A method, comprising:

forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level; and

performing an ion implant process using at least said gate electrode as a mask to implant a dopant material into said bulk substrate, said implant process being performed with a dopant material that is of the same type as said dopant material in said substrate, said implant process resulting in first, second and third doped regions formed in said bulk substrate, said first doped region being substantially aligned with said gate electrode and vertically spaced apart from said second and third doped regions, said first, second and third doped regions having a dopant concentration level that is greater than said first concentration level.

61. The method of claim 60, wherein forming a gate electrode comprises forming a gate electrode comprised of polysilicon.

62. The method of claim 60, wherein forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level, comprises forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate comprised of silicon, a buried oxide layer comprised of silicon dioxide and an active layer comprised of silicon, said bulk substrate being doped with a dopant material at a first concentration level.

63. The method of claim 60, wherein forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level, comprises forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a P-type dopant material at a first concentration level of approximately 10^{15} ions/cm^3.

64. The method of claim 60, wherein forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with a dopant material at a first concentration level, comprises forming a gate electrode above a silicon-on-insulator substrate comprised of a bulk substrate, a buried oxide layer and an active layer, said bulk substrate being doped with an N-type dopant material at a first concentration level of approximately 10^{15} ions/cm^3.

65. The method of claim 60, wherein said first, second and third doped regions have a dopant concentration level of at least approximately 10^{16} ions/cm^3.

66. The method of claim 60, wherein performing said ion implant process results in said first, second and third doped regions each having a thickness of approximately 10-50 nm.

67. The method of claim 60, further comprising forming a source region, a drain region and a plurality of conductive contacts.

68. The method of claim 60, wherein said first doped region is vertically spaced apart from said second and third doped regions by a distance that approximately corresponds to a thickness of said gate electrode.

69. The method of claim 60, wherein said second and third doped regions each have an upper surface, said upper surface of each of said second and third doped regions being positioned below an interface between said buried oxide layer and said bulk substrate by a distance that approximately corresponds to a thickness of said gate electrode.

70. The method of claim 60, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate, said second and third doped regions each having an upper surface, said upper surface of each of said second and third doped regions being positioned below an

interface between said buried oxide layer and said bulk substrate by a distance that approximately corresponds to a thickness of said gate electrode.

71. The method of claim 60, wherein performing said ion implant process results in said first, second and third doped regions each having a thickness of approximately 10-50 nm.

72. The method of claim 60, further comprising performing at least one anneal process at a temperature ranging from approximately 600-1050°C after said ion implant process is performed.

73. The method of claim 60, wherein performing said ion implant process comprises performing said ion implant process at an energy level ranging from approximately 40-400 keV.

74. The method of claim 60, wherein performing said ion implant process comprises performing said ion implant process with a dopant dose that ranges from approximately $1e^{14}$-$1e^{16}$ ions/cm^2.

75. The method of claim 60, wherein said first doped region has an upper surface that is positioned approximately 0-5 nm below an interface between said buried oxide layer and said bulk substrate.

76. The method of claim 60, further comprising forming a source region, a drain region and a plurality of conductive contacts.